IN THE CLAIMS:

Claims 1-9 are currently pending in the present application.

Please amend Claims 1 and 4-9 as set forth below.

1. (Once Amended) A method of forming gates in a semiconductor device having a non-linear top profile, the method comprising the steps of:

forming a dummy gate insulating layer on a semiconductor substrate having a field oxide layer isolating the device;

depositing a dummy gate polysilicon layer and a hard mask layer on the dummy gate insulating layer sequentially;

patterning the hard mask layer into a mask pattern and patterning the dummy gate polysilicon layer and the dummy gate insulating layer using the mask pattern as an etch barrier, creating a plurality of patterned dummy gate polysilicon and insulating layers each having sidewalls, wherein the patterned dummy gate polysilicon and insulating layers are formed on the semiconductor substrate and on the field oxide layer;

forming spacers at the sidewalls of the patterned dummy gate polysilicon and insulating layers;

depositing an insulating interlayer on the resultant structure after forming the spacers;

exposing a surface of the patterned dummy gate polysilicon and insulating layers by carrying out an oxide layer chemical mechanical polishing (CMP) process utilizing a first high selection ratio sufficient

to polish the insulating layer but insufficient to polish the patterned dummy gate polysilicon and insulating layers;

forming a damascene structure by removing the patterned dummy gate polysilicon and insulating layers using the insulating interlayer as another etch barrier;

depositing a gate insulating layer and a gate metal layer on the entire surface of the semiconductor substrate having the damascene structure; and

exposing a surface of the insulating interlayer by carrying out a metal CMP process utilizing a second high selection ratio sufficient to polish the metal layer but insufficient to polish the insulating interlayer.

4. (Once Amended) The method of claim 1, wherein the first high selection ratio between the insulating interlayer and the dummy gate polysilicon layer is over 20.

5. (Once Amended) The method of claim 1, wherein the insulating interlayer CMP utilizes a slurry including CeO_2 particles.

6. (Once Amended) The method of claim 5, wherein the pH of the slurry, including CeO_2 particles, is between 3 and 11.

7. (Once Amended) The method of claim 1, wherein the second high selection ratio between the insulating interlayer and the gate metal layer is over 50.

8. (Once Amended) The method of claim 1, wherein the metal CMP uses a slurry for the metal layer.

9. (Once Amended) The method of claim 8, wherein the pH of the slurry for the metal layer is between 2 and 7.